TSMC-02-150

January 5, 2004

To: Commissioner for Patents
P.O.Box 1450
Alexandria, VA 22313-1450

Fr: George O. Saile, Reg. No. 19,572
28 Davis Avenue
Poughkeepsie, N.Y. 12603

Subject: Serial No. 10/697,833 10/30/03

Juing-Yi Cheng et al.

A METHOD OF IMPROVING SHORT CHANNEL EFFECT AND GATE OXIDE RELIABILITY BY NITROGEN PLASMA TREATMENT BEFORE SPACER DEPOSITION

INFORMATION DISCLOSURE STATEMENT

Enclosed is Form PTO-1449, Information Disclosure Citation In An Application.

The following Patents and/or Publications are submitted to comply with the duty of disclosure under CFR 1.97-1.99 and 37 CFR 1.56.

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on January 27, 2004.

Stephen B. Ackerman, Reg.# 37761

Signature/Date 1/27/04

U.S. Patent 5,808,348 to Ito et al., "Non-Uniformly Nitrided Gate Oxide and Method," discloses a nitrided gate oxide process.

U.S. Patent 6,373,113 to Gardner et al., "Nitrogenated Gate Structure for Improved Transistor Performance and Method for Making Same," discloses a nitrogenated gate structure and method.

U.S. Patent 5,990,517 to Irino, "Semiconductor Memory Device Containing Nitrogen in a Gate Oxide Film," discloses a process to introduce nitrogen into a gate dielectric.

U.S. Patent 5,872,049 to Gardner et al., "Nitrogenated Gate Structure for Improved Transistor Performance and Method for Making Same," discusses an integrated circuit fabrication method incorporating nitrogen into the polysilicon-dielectric interface in an MOS transistor.

U.S. Patent 5,567,638 to Lin et al., "Method for Suppressing Boron Penetration in PMOS with Nitridized Polysilicon Gate," discusses a method for suppressing boron penetration in a PMOS with a nitridized polysilicon gate.

U.S. Patent 5,189,504 to Nakayama et al., "Semiconductor Device of MOS Structure Having P-Type Gate Electrode," discusses a semiconductor device of a MOS structure having a p-type gate electrode which has a gate electrode including at least two layers consisting of a boron-doped polysilicon layer and a polysilicon layer doped with aboron and an inert material.

Sincerely,

Stephen B. Ackerman,
Reg. No. 37761

Form PTO-1449

INFORMATION DISCLOSURE CITATION IN AN APPLICATION

(Use several sheets if necessary)

Docket Number (Optional)	Application Number
TSMC-02-150	10/697,833
Applicant: Juing-Yi Chang et al.	
Filing Date: 10/30/03	Group Art Unit:

U. S. PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
	5808348	9/15/98	Ito et al.	257	410	6/27/97
	6373113	4/16/02	Gardner et al.	257	411	5/6/98
	5990517	11/23/99	Irino	257	339	8/27/97
	5872049	2/16/99	Gardner et al.	438	585	6/19/96
	5567638	10/22/96	Lin et al.	437	46	6/14/95
	5189504	2/23/93	Nakayama et al.	257	422	1/30/92

FOREIGN PATENT DOCUMENTS

	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	Translation YES	Translation NO

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

EXAMINER	DATE CONSIDERED

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP § 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to the applicant.